WHAT IS CLAIMED IS:

1. A switch for a network comprising:

a memory mechanism in which portions of packets are stored; and

a mechanism for instituting changes to the memory mechanism while the memory mechanism continuously operating on packets.

2. A switch as described in Claim 1 wherein the memory mechanism includes a plurality of memory controllers.

3. A switch as described in Claim 2 wherein the instituting mechanism includes a command buffer disposed in each memory controller in which changes to the memory controller are stored until the changes are implemented.

4. A switch as described in Claim 3 including a fabric in which the memory mechanism and the instituting mechanism are disposed, and wherein the instituting mechanism includes an MCP disposed in the fabric connected to the command buffer of each memory controller in the fabric, the MCP sends the changes to the buffer.

5. A switch as described in Claim 4 wherein each memory controller institutes changes in its command buffer at a same logical clock cycle when a the memory controller receives an implementation signal.

6. A switch as described in Claim 5 wherein the fabric has an aggregator which receives the implementation signal and sends it to the memory controllers.

7. A switch as described in Claim 6 including a plurality of fabrics.

8. A switch as described in Claim 7 including a port card which receives the implementation signal from the network and sends the implementation signal to each fabric in the switch.

9. A switch as described in Claim 8 wherein the port card includes a striper and an unstriper, and the fabric includes a separator, the striper sending the implementation signal to the aggregator of each fabric as a stripe, and the unstriper receiving any data from the separator of each fabric as a stripe.

10. A method for switching packets comprising:

receiving changes for a memory mechanism of a switch at a buffer of the switch; and

implementing the changes to the memory mechanism when the memory mechanism receives an implementation signal while the memory mechanism continuously operates on packets.

11. A method as described in Claim 10 wherein the buffer includes a command buffer and the receiving step includes the step of receiving changes for each memory controller of each fabric at the command buffer.

12. A method as described in Claim 11 including before the receiving step, there is the step of sending the changes to each command buffer from the MCP of the fabric.

13. A method as described in Claim 12 wherein the implementing step includes the step of implementing the changes to all the memory controllers of all the fabrics at a same logical clock cycle.

14. A method as described in Claim 13 including before the implementing step, there is the step of receiving the implementation signal at the switch in a receive message packets.

15. A method as described in Claim 14 wherein the implementation receiving step includes the step of receiving the receive message packet at a port card of the switch.

16. A method as described in Claim 15 including after the packet receiving step, there is the step of sending the implementation signal with a striper of the port card as a stripe to an aggregator of each fabric of the switch.

17. A method as described in Claim 16 including after the implementation sending step, there is the step of transferring the implementation signal from the aggregator to each memory controller.